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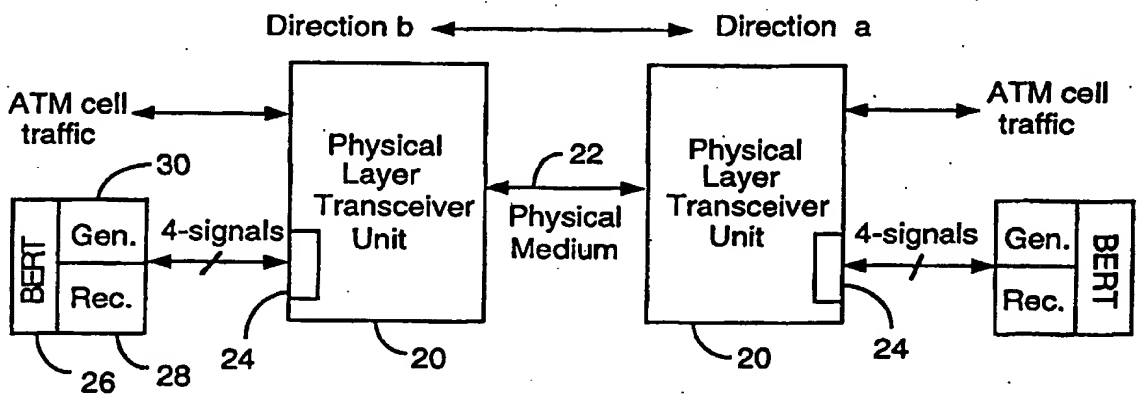

(57) Abstract

Telecommunications networks require a variety of tests to monitor their proper operations. Performance monitoring (and fault detection) of the physical layer of a transmission system is one of them and is usually accomplished by using a bit error rate test (BERT). The BERT of the invention uses modified ATM idle cells to conduct one–way, bidirectional and loopback BERT. ATM idle cells are loaded with BERT data at the transmit end and recovered at the receive end. The BERT data are processed according to the different data rates of the ATM transmission system. Performance parameters are derived from the received BERT data. The disclosure describes a method as well as a system for performing such a test.

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PERFORMANCE MONITORING OF AN ATM NETWORK

Field of Invention

The invention generally relates to a performance test of a telecommunications network. In particular, it is directed to a technique of measuring performance parameters of such a network.

Background of Invention

Telecommunications networks require a variety of methods to monitor the system performance. One common method of performance monitoring and fault detection of the physical layer of a transmission system is the bit error rate test (BERT). BERT is conducted in the direction of transmission but there are several modes of BERT. In order to sectionalize performance faults, it is useful to verify one-way error rate performance (i.e. from the transmit-end to the receiver-end, called one-way BERT). There is also bidirectional BERT in which one-way BERT is conducted in two opposite directions simultaneously. Another mode is a loopback test (called loopback BERT) in which a looped back performance test is originated from either end of the system with a loopback established at the opposite end of the system.

There are some standard bit error rate test sets available in the art. These commercially available BERT sets contain a generator section and a receiver section. The generator section outputs a serialized data pattern which may be fixed or pseudo-randomized. The receiver section receives a serialized data pattern and verifies it for errors with respect to an expected receive pattern. The generator and receiver sections generally operate independently allowing one-way testing using two BERT sets or looped back testing using a single BERT set. The BERT receiver section also usually contains performance monitoring capabilities by providing error statistics. The BERT set normally provides various interfaces for connection to the generated and received data.

This invention allows the use of a standard bit error rate test set for monitoring the performance of the physical layer of an ATM cell-based transmission system by using a simple 4-signal interface consisting of data to the BERT receiver, data from the BERT generator,

and clocks to the generator and the receiver (2 clocks). The invention utilizes the idle cell structure of the physical layer to transport BERT data to conduct a transmission performance test.

Objects of Invention

It is therefore an object of the invention to provide a method of and system for monitoring the performance of an ATM network.

It is another object of the invention to provide a method of and system for monitoring the performance of an ATM network by using ATM idle cells.

It is a further object of the invention to provide a method of and system for conducting BERT on an ATM network.

It is still another object of the invention to provide a method of and system for conducting BERT on an ATM network in several different modes.

It is yet a further object of the invention to provide a method of and system for conducting BERT on an ATM network using ATM idle cells.

It is another object of the invention to provide a method of and system for conducting BERT on an ATM network in a mode with asymmetric system data rates.

Summary of invention

Briefly stated, the invention is directed to a method of conducting a performance test in an ATM network. The method comprises steps of sending from a first node in the ATM network a series of ATM test cells which contain a series of bits arranged in a test pattern and receiving at a second node the series of ATM test cells. The method further includes a step of deriving a performance parameter of the network from the received test pattern. In one embodiment, the series of bits arranged in a test pattern are BERT data.

According to another aspect, the invention is directed to a method of conducting a transmission performance test between nodes in an ATM network. The method comprises steps of generating ATM idle cells, generating BERT data and inserting BERT data in one or more ATM idle cells to generate one or more modified ATM idle cells. The method further includes steps of sending the one or more

modified ATM idle cells through the ATM network under test, receiving the one or more modified ATM idle cells, and deriving a transmission performance parameter of the network from received BERT data in the one or more received modified ATM idle cells.

According to yet a further aspect, the invention is directed to a system for conducting a performance test between nodes in an ATM network. The system comprises a test pattern generator for generating a series of bits arranged in a test pattern and an idle cell generator for generating a series of ATM idle cells and inserting therein the series of bits arranged in the test pattern to generate a series of modified ATM idle cells. The system also includes a test pattern insertion MUX for transmitting the series of modified ATM idle cells through the ATM network under test.

Brief description of the Drawings

Figure 1 shows a standard ATM idle cell format;

Figure 2 shows a modified ATM idle cell format according to an embodiment of the invention;

Figure 3 is a block diagram of a BERT arrangement in one-way BERT mode according to one embodiment;

Figure 4 is a schematic block diagram of a transmit end according to one embodiment;

Figure 5 is a schematic block diagram of a receive end according to one embodiment;

Figure 6 is a block diagram of a BERT arrangement in a loopback mode according to one embodiment;

Figure 7 shows a way to arrange Figures 8 and 9;

Figure 8 is a schematic block diagram of a transmit-receive end in the loopback mode according to one embodiment; and

Figure 9 is a schematic block diagram of a loopback end in the loopback mode according to one embodiment.

Detailed Description of Preferred Embodiments of the Invention

During ATM communication, idle cells are employed to decouple the ATM cell traffic rate from payload capacity of the specific transmission system used by the physical layer. In other words, the transmit end inserts idle cells into the data stream when no ATM cell

traffic is available. The receive end detects the idle cells by decoding the unique header field and extracts them from the data stream without passing them to the ATM layer.

According to the present invention, BERT data are delivered to the ATM system under test by using a specially modified ATM idle cell. As shown in Figure 1, a standard ATM idle cell consists of a fixed 5 octet header followed by a payload of 48 octets fixed with a value of $6A.

According to the embodiment, BERT data are substituted for the fixed 48 payload octets of the idle cell and are delivered to the system. Thus the modified idle cell appears as shown in Figure 2. During BERT mode, the ATM cell traffic is interrupted and only the modified idle cells carrying BERT data are transmitted.

As described earlier BERT can be conducted in several modes and some preferred embodiments will be described in detail below.

<u>One-Way BERT</u>

Overview

One-way BERT is used to measure the physical layer one-way performance at each receiver of the transmission system. Figure 3 illustrates schematically the configuration required for testing two simultaneous one-way performances. The Physical Layer Transceiver Units (PLTU) 20 are the equipment providing the physical layer functionality for the ATM cell traffic at both ends of a bidirectional transmission system through a physical medium 22, e.g. wire, fiber optic wireless, etc. Through a BERT interface 24, each PLTU is connected to a BERT set 26 providing test pattern generator 28 and receiver functions 30. For the bidirectional BERT, four interface signals are used between the BERT set and the PLTU at each end of the system. They are Tx Data, Tx Clk, Rx Data, Rx Clk. The following three one-way configurations are possible:

Direction a BERT, direction b normal ATM traffic;
Direction b BERT, direction a normal ATM traffic;
Bidirectional a and b BERT, no ATM traffic.

For PLTUs that provide independent data randomization or scrambling on the transmission loop, the pseudo-random patterns typically used for BERT are not necessary. In this case, the separate BERT generator functions are not required. During the BERT mode, the transmitted traffic consists of unmodified idle cells containing $6A data. The receiver is connected to a BERT set with a BERT receiver only, which is configured to compare the received data to the expected $6A pattern.

Instead of providing an interface to connect the ATM modems to external BERT sets, the BERT generator and receiver functions may be entirely implemented within the PLTUs. This would provide an integrated BERT capability providing self-contained BERT without the need for external test equipment.

Figure 4 is a block diagram of a circuit used in the transmit end of the one-way BERT according to one embodiment. The figure includes BERT generator 40 which produces BERT data under control of a BERT clock signal from BERT clock generator 42. An idle cell generator 44 produces ATM idle cells and also inserts the BERT data generated by the BERT data generator in their payload fields to create modified idle cells. A BERT insertion MUX 46 halts ATM cell traffic and transmits the modified idle cells for an ATM system under test. One-way BERT can be performed in the ATM system in direction a or b, or both directions simultaneously, as shown in Figure 3. At the transmit end, the source of BERT data is a commercially available BERT set which generates a self-synchronizing pseudo-random serial data pattern, according to a BERT clock provided by the circuit. The idle cell generator circuit receives cell boundary and timing information from the ATM system under test. It constructs the modified idle cell by producing the fixed header octets at the appropriate time in the system, then capturing BERT data from the BERT set and transmitting the data as the 48 payload octets. This process is repeated for the duration of the BERT test. For the case where a commercially available BERT set is not used at the transmit end, the idle cell generator constructs a standard ATM idle cell as shown in Figure 1 and relies on the ATM system for randomization.

The BERT clock generator 42 produces a clock at the frequency of the direction a or b bit transmission rate (r_a or r_b, respectively) of the

ATM system under test. The idle cell generator 44 provides control signals to the BERT clock generator circuit to gap the BERT clock while header octets are produced and while other non-ATM overhead data are being transmitted by the system.

During the BERT test procedure, ATM traffic directed to the system under test is preempted by the modified idle cells from the idle cell generator. The BERT mode control signal 48 is used in conjunction with the BERT insertion MUX 46 to feed the output of the idle cell generator to the ATM system for the duration of the test.

Referring to Figure 5, at the receive end, the modified idle cells are terminated by a circuit which includes a cell payload extractor circuit 50 which strips the cell header and extracts the payload under control of a cell delineator 52. A BERT clock generator 54 is also under control of a cell delineator. The cell payload extractor circuit extracts the payload BERT data and sends them to the BERT receiver. The BERT receiver can be a commercially available BERT set which is programmed to accept the same self-synchronizing pseudo-random serial data pattern that is being sent by the transmitting BERT set. In the case where no transmit BERT set is used, the receive BERT set is programmed to accept the standard ATM idle cell payload value of $6A.

Because bit errors may be present in the modified idle cell header, no assumptions are made regarding the contents of the header. Thus it is imperative that ATM traffic is suspended during the BERT test so that bit errors in the modified idle cell header are not misinterpreted as valid ATM traffic by the system. Accordingly, all received cells are treated as modified idle cells, thus the payload data of all received cells is transmitted to the BERT set.

Timing information for the circuit is provided by the ATM system under test. A cell delineator circuit recovers cell boundary information from the received data stream by using the Header Error Control field according to International Telecommunications Union Standard I.432. The cell delineator uses the cell boundary information to derive circuit control signals.

The modified idle cell payload containing the BERT data is extracted from the incoming cell stream based on control information provided from the cell delineator. The extracted BERT data is output

from the circuit as a serial stream to the BERT set. The BERT set receives data according to a BERT clock provided by the BERT clock generator circuit. The frequency of the BERT clock is equal to that of the bit transmission rate of the ATM system under test. Control information from the cell delineator is used to gap the BERT clock during header octets and while other non-ATM data is being transmitted by the system.

Loopback BERT

Overview

For bidirectional transmission with symmetrical data rates in both directions, a loopback can be implemented by simply extracting the BERT data from the idle cells received at the far-end and inserting the same data into the transmitted idle cells. However, many transmission systems support asymmetrical transmission rates. For an asymmetrical system, a physical layer BERT using idle cells may be implemented by employing a lower payload rate that is common to both directions of transmission. One method to implement this is to use the highest common factor (HCF) rate between the two ATM payload rates. Let the transmission rate of direction a be r_a, and the transmission rate for direction b be r_b.

For the case where r_a is an integer multiple of r_b or vice versa, $HCF(r_a,r_b)$ is simply the lower of the two rates. Therefore the loopback BERT uses a rate equal to the lower rate. For the case where r_a and r_b are not direct integer multiples of each other, the loopback BERT uses a rate equal to the highest common factor between the two rates, $HCF(r_a,r_b)$. For example, a transmission rate of 1 Mbps would be used for a loopback BERT with a system providing asymmetrical payload rates of $r_a = 3$ Mbps and $r_b = 2$ Mbps.

Figure 6 shows the configuration for loopback at the far-end to support testing with an external BERT set located at the other end. BERT may be performed from either end of the system.

Implementation

Figures 8 and 9 arranged in the fashion shown in Figure 7 illustrate a block diagram of a circuit used to implement loopback

BERT, according to one embodiment. This implementation requires transmit and receive circuits to be located at one end of the ATM system under test, with circuitry to loopback the BERT data at the far end.

The transmit circuit shown in Figure 8 operates in an identical fashion to the one-way implementation described above except for the addition of a repeater circuit 80. The repeater functions to receive each bit from the BERT set 82 and repeat it by the factor s_a, where

$$Sa = \frac{ra}{HCF(ra, rb)}$$

The repeated bits are then presented to the idle cell generator which inserts them into the modified idle cell payload. The BERT clock generator 84 supplies a gapped clock to the BERT set at a rate of HCF(ra,rb). For the case where a transmit BERT set is not used, the repeater generates the fixed \$6A value with each bit repeated s_a times.

At the loopback end shown in Figure 9, the modified idle cells are terminated in the same manner as the one-way implementation except for the addition of a bit sampler 100 and loopback elastic buffer. Again, because bit errors may be present in the modified idle cell header, all received cells are treated as modified idle cells and all payload data are fed to the bit sampler. Also, ATM traffic is suspended during the BERT test so that bit errors in the modified idle cell header are not misinterpreted as valid ATM traffic by the system.

The bit sampler restores the data rate of HCF(r_a,r_b) by sampling every s_ath bit from the extracted payload data, thus restoring the BERT data produced at the transmit end before the repeater circuit 102. The restored BERT data from the sampler is then queued into an elastic buffer 104. The buffer serves to re-time the BERT data to the return direction b data rate r_b. The elastic buffer must be sized to accommodate the maximum anticipated duration of non-payload traffic in both directions in the ATM system under test.

BERT data stored in the elastic buffer are dequeued under the control of the return transmit idle cell generator. The dequeued BERT data is again fed to a repeater circuit 102, which repeats each bit of the BERT data by the factor sb, where

$$Sb = \frac{rb}{HCF(ra, rb)}$$

The repeated BERT data is then presented to the idle cell generator 106 for insertion into modified idle cells for transmission on the return path of the ATM system under test. The receiver in the return path operates identically to the receiver at the loopback end. All received cells are terminated with no assumptions regarding the cell header contents and with ATM traffic suspended. The extracted payload is fed to a bit sampler circuit 86 which restores the data rate of HCF(ra,rb) by sampling every s_bth bit from the extracted payload data, thus restoring the original BERT data.

The receive BERT set receives the restored data according to a BERT clock provided by the BERT clock generator circuit. The frequency of the BERT clock is equal to HCF(ra,rb). Control information from the cell delineator is used to gap the BERT clock during header octets and while other non-ATM data are being transmitted by the system.

WHAT IS CLAIMED IS:

1. In an ATM network, a method of conducting a performance test between a first node and a second node comprising steps of:

sending from the first node a series of ATM test cells which contain a series of bits arranged in a test pattern;

receiving at the second node the series of ATM test cells; and

deriving a performance parameter of the network from the received test pattern.

2. The method according to claim 1 wherein the series of ATM test cells comprise ATM idle cells.

3. The method according to claim 2 wherein the ATM idle cells contain BERT data.

4. In an ATM network, a method of conducting a transmission performance test between nodes comprising steps of:

generating ATM idle cells;

generating BERT data;

inserting BERT data in one or more ATM idle cells to generate one or more modified ATM idle cells;

sending the one or more modified ATM idle cells through the ATM network under test;

receiving the one or more modified ATM idle cells; and

deriving a transmission performance parameter of the network from received BERT data in the one or more received modified ATM idle cells.

5. The method of conducting a transmission performance test according to claim 4 wherein the test is performed in either one or both of the two opposite directions between the nodes.

6. The method of conducting a transmission performance test according to claim 5, wherein the test is performed in the two opposite directions between the nodes, comprising a further step of:

elastically buffering and looping back one or more modified ATM idle cells at one of the nodes.

7. The method of conducting a transmission performance test according to claim 6, wherein directions a and b are the two opposite directions between the nodes, and r_a and r_b are transmission rates for directions a and b respectively, comprising a further step of:

adjusting the rates of BERT data in either one or both directions to a common rate

8. The method of conducting a transmission performance test according to claim 7, comprising a further step of:

repeating the BERT data by factor s_a in direction a where

$$s_a = \frac{r_a}{HCF(r_a, r_b)}$$

and $HCF(r_a, r_b)$ is the highest common factor between r_a and r_b.

9. The method of conducting a transmission performance test according to claim 8, comprising a further step of:

sampling the repeated BERT data by factor s_a to generate the received BERT data.

10. The method of conducting a transmission performance test according to claim 7, comprising a further step of:

repeating the BERT data by factor s_b in direction b where

$$s_b = \frac{r_b}{HCF(r_a, r_b)}$$

and $HCF(r_a, r_b)$ is the highest common factor between r_a and r_b.

11. The method of conducting a transmission performance test according to claim 10, comprising a further step of:

sampling the repeated BERT data by factor s_b to generate the received BERT data.

12. A system for conducting a performance test between nodes in an ATM network, comprising:

a test pattern generator for generating a series of bits arranged in a test pattern;

an idle cell generator for generating a series of ATM idle cells and inserting therein the series of bits arranged in the test pattern to generate a series of modified ATM idle cells; and

a test pattern insertion MUX for transmitting the series of modified ATM idle cells through the ATM network under test.

13. The system for conducting a performance test between nodes according to claim 12 wherein the test pattern generator comprises a BERT data generator.

14. The system for conducting a performance test between nodes in an ATM network, according to claim 12 further comprising:

a cell payload extractor circuit for extracting the series of modified ATM idle cells to generate a series of received bits arranged in the received test pattern; and

a test pattern receiver for generating performance parameters from the series of received bits arranged in the received test pattern.

15. The system for conducting a performance test between nodes according to claim 14 wherein the test pattern receiver comprises a BERT data receiver.

16. The system for conducting a performance test between nodes according to claim 15, further comprising an elastic buffer for buffering and looping back a series of modified ATM idle cells.

17. The system for conducting a performance test between nodes according to claim 16, further comprising a repeater and a sampler for accommodating different transmission rates in the two opposite directions.

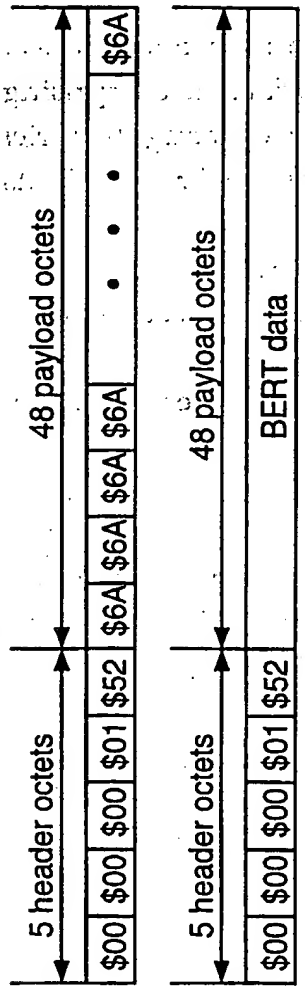


Fig 1

Fig 2

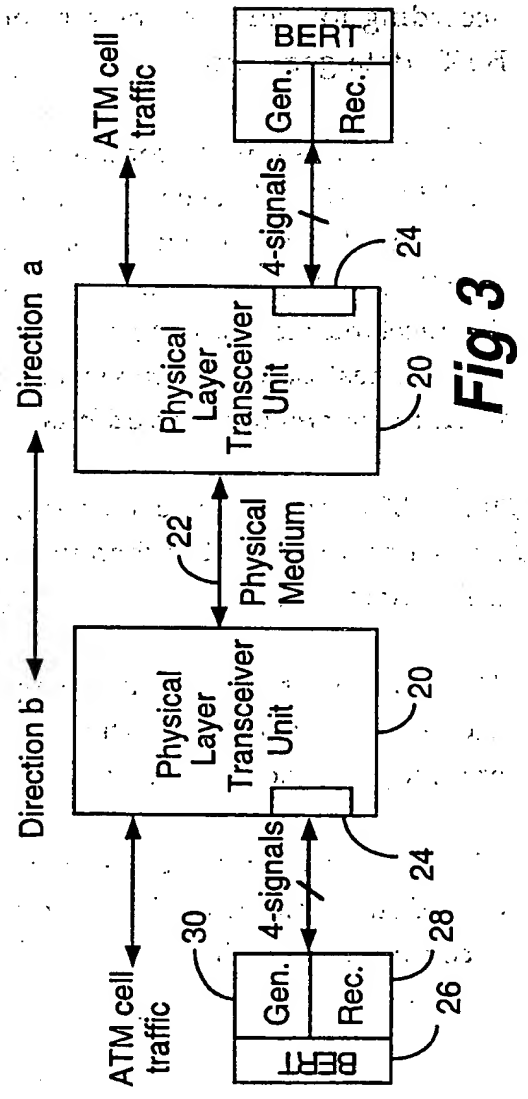
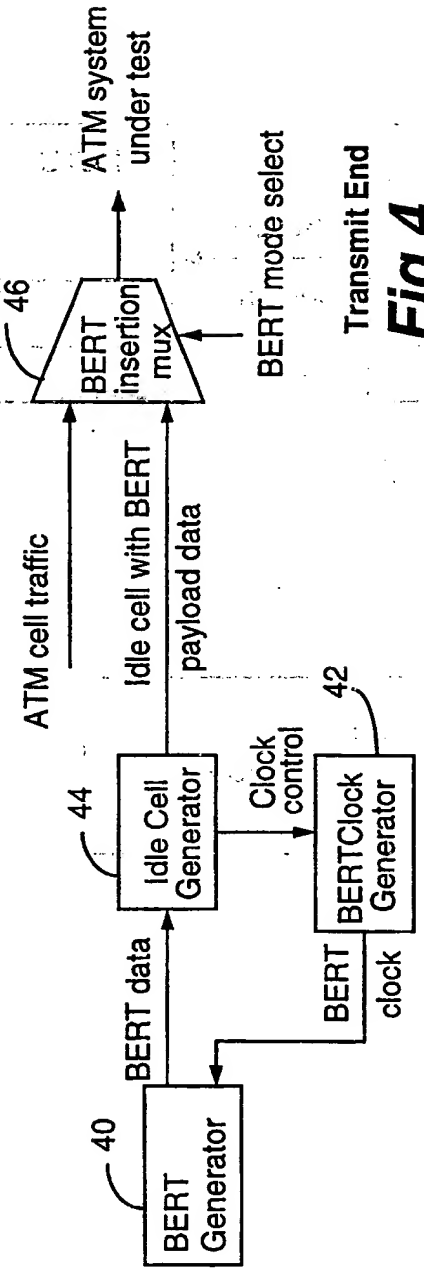
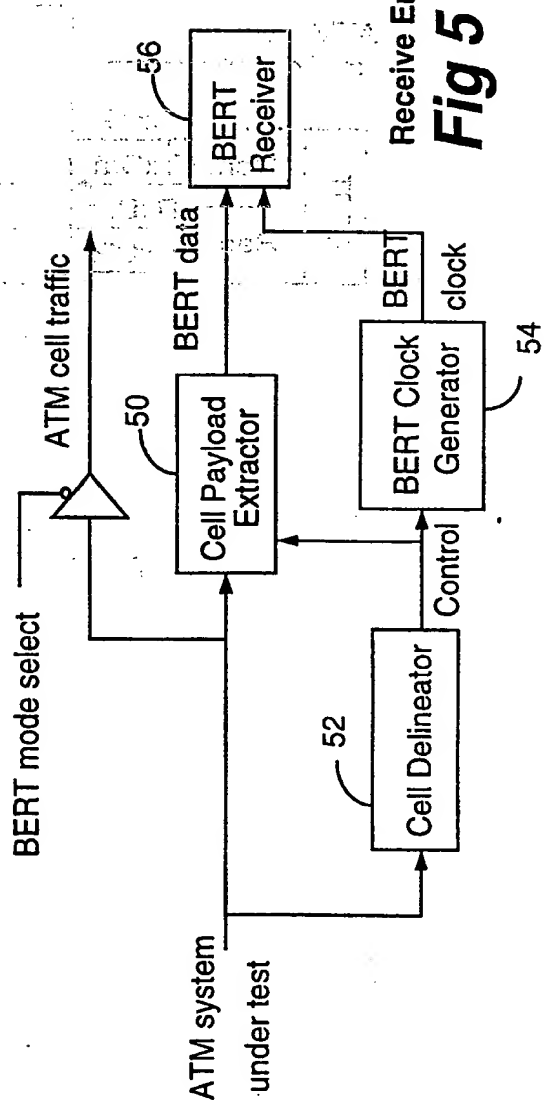


Fig 3



Transmit End

Fig 4



Receive End

Fig 5

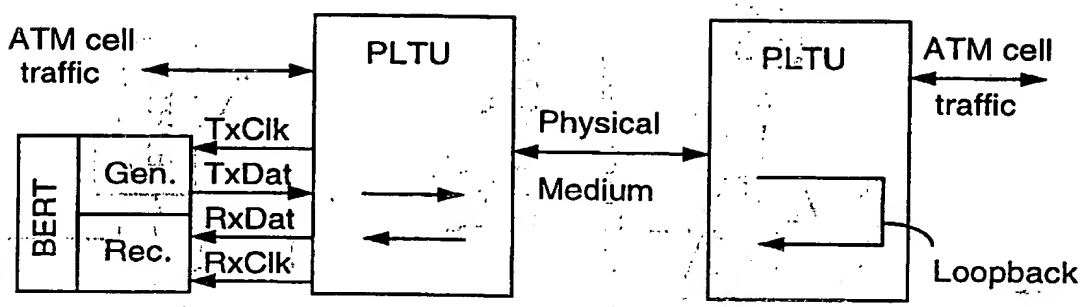


Fig 6

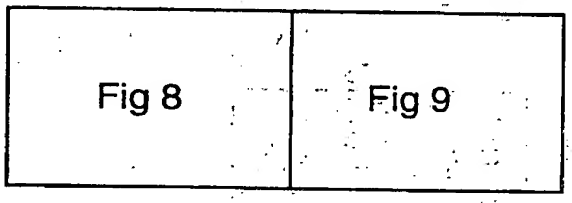


Fig 7

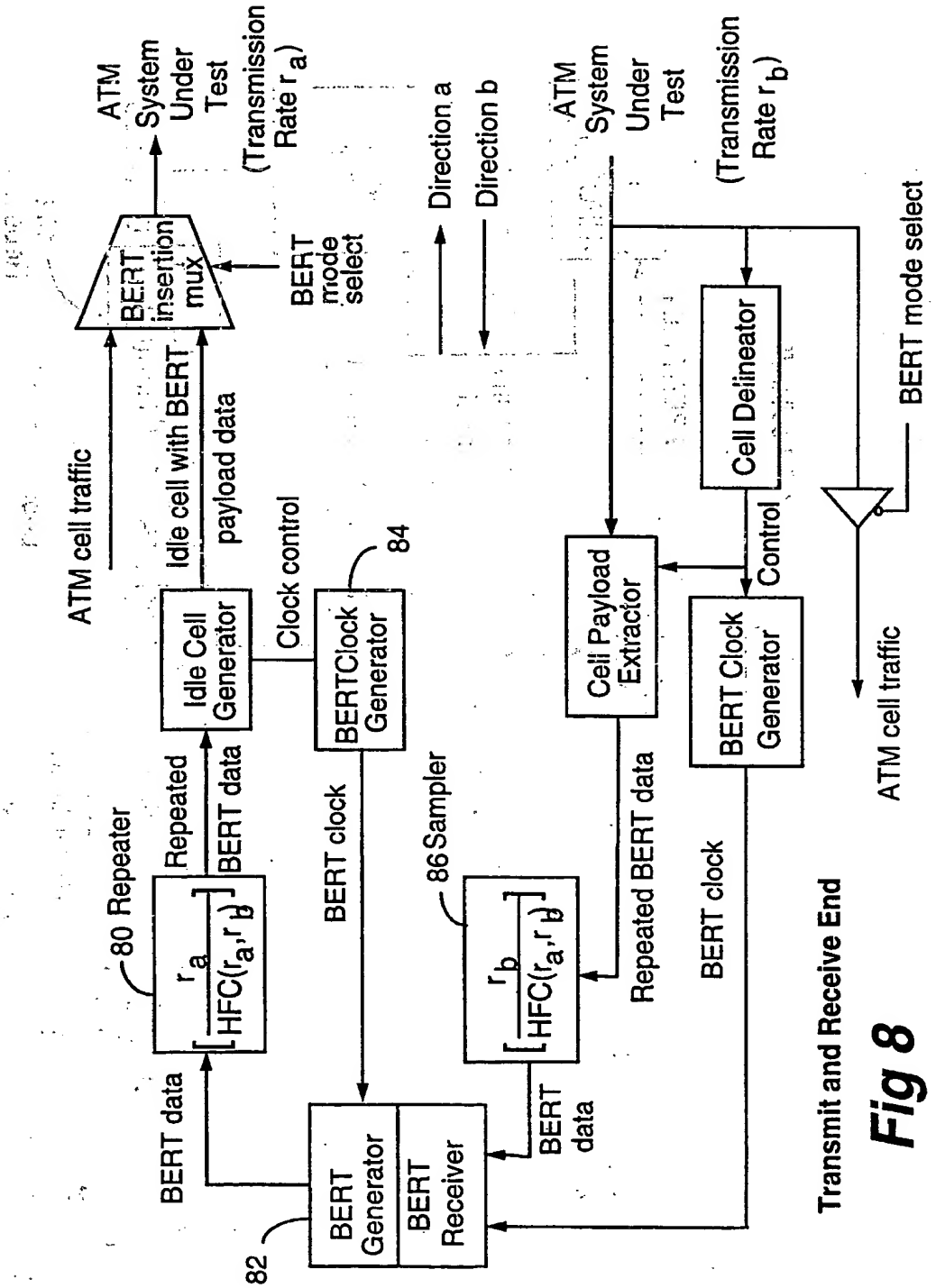


Fig 8

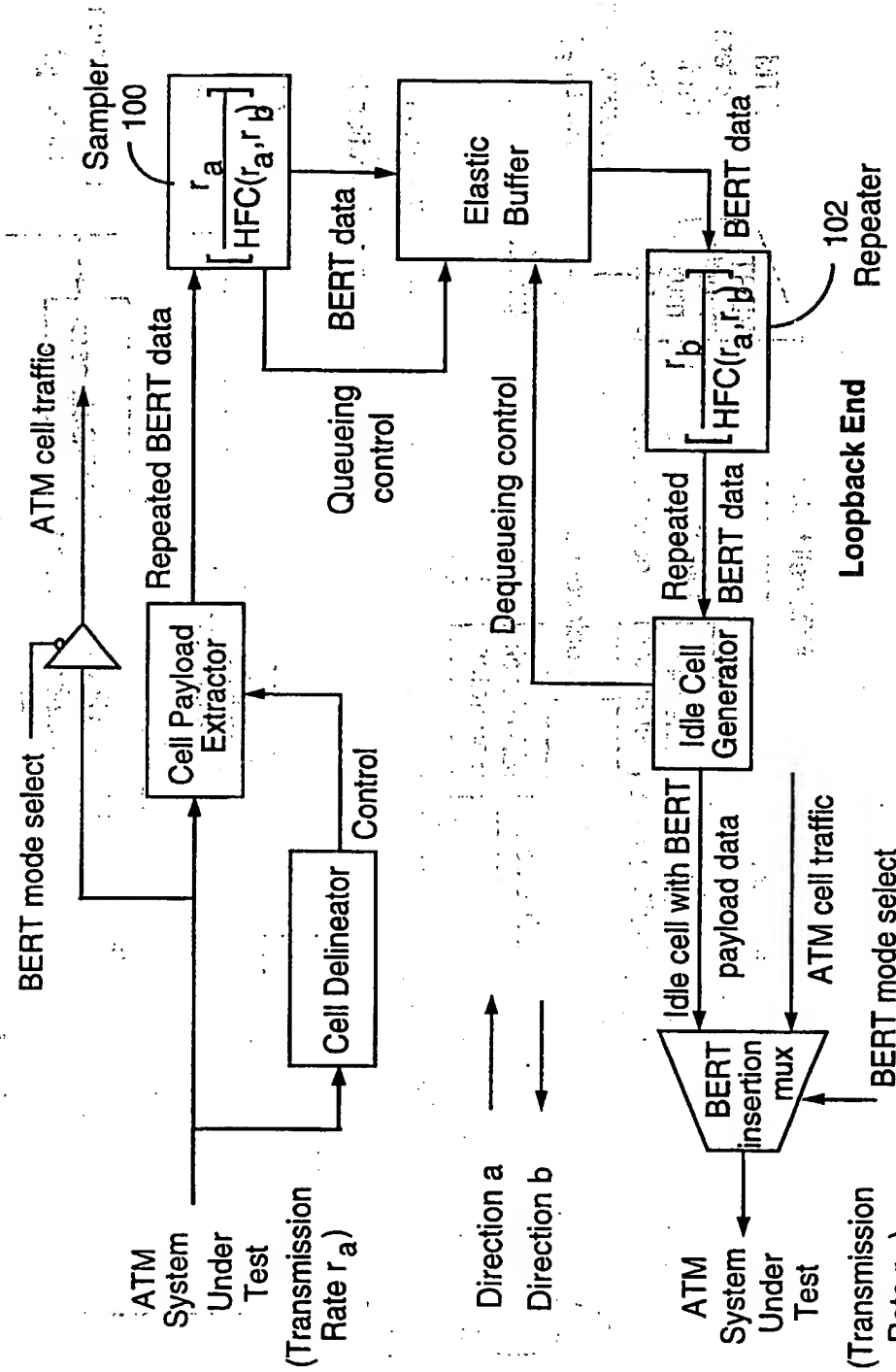


Fig 9

INTERNATIONAL SEARCH REPORT

Inter onal Application No
PCT/CA 98/00087

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04Q11/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04Q H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DUFF J A: "TEST CHALLENGES OF ATM" ANNUAL REVIEW OF COMMUNICATIONS, vol. 46, 1 January 1993, pages 320-328, XP000321941 paragraphs "Background to ATM testing"; "Physical Layer Tests" ---	1-5, 12-15
A	KEISER G ET AL: "TEST TRAFFIC GENERATION EQUIPMENT AND ALGORITHMS FOR EVALUATING ATMNETWORKS" COMPUTER COMMUNICATIONS, vol. 19, no. 12, October 1996, pages 962-971, XP000635579 ---	1-5, 12-15
A	EP 0 667 694 A (FRANCE TELECOM) 16 August 1995 see abstract see column 2, line 32 - column 3, line 12 --- -/--	1,4,12

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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1

Date of the actual completion of the international search	Date of mailing of the international search report
18 May 1998	29/05/1998

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INTERNATIONAL SEARCH REPORT

Inte. ional Application No
PCT/CA 98/00087

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